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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known Application Number TBD Filing Date Herewith First Named Inventor Yeo, et al. Art Unit TBD Examiner Name TBD Attorney Docket Number TSM03-0511		
Sheet	1	of	1			
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
[Signature]	A	US-6,252,284 B1	06-26-2001	Muller, et al.	/	
[Signature]	B	US-6,391,695 B1	05-21-2002	Yu		
[Signature]	C	US-6,391,782 B1	05-21-2002	Yu		
[Signature]	D	US-6,413,802 B1	07-02-2002	Hu, et al.		
[Signature]	E	US-6,432,829 B1	08-13-2002	Muller, et al.		
[Signature]	F	US-6,451,658 B1	09-17-2002	Yu, et al.		
[Signature]	G	US-6,492,212 B1 US-	12-10-2002	leong, et al.		
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
[Signature]	H	HUANG, X., et al. "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5 (May 2001) pp. 880-886.				
[Signature]	I	YANG, F.L., et al. "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, (June 2002) pp. 109-110.				
[Signature]	J	WONG, H.-S.P. "Beyond the Conventional Transistor," IBM Journal of Research and Development (March/May 2002) pp. 133-167.				
[Signature]	K	CHAU, R., et al. "Advanced Depleted-Substrate Transistors: Single-gate, Double-gate and Tri-gate," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, (2002) pp. 68-69.				
[Signature]	L	YANG, F.L., et al. "25nm CMOS Omega FETs," International Electron Devices Meeting, Digest of Technical Papers, (December 2002) pp. 255-258.				
[Signature]	M	COLINGE, J.P., et al. "Silicon-on-Insulator "Gate -All-Around Device,"" International Electron Devices Meeting, (1990) pp. 595-598.				
[Signature]	N	LEOBANDUNG, E. "Wire-Channel and wrap-around-gate metal-oxide-semiconductor field-effect transistors with a significant reduction of short channel effects," Journal of Vacuum Science and Technology, Vol. B15, No. 6, (November/December 1997) pp. 2791-2794.				
Examiner Signature	[Signature]			Date Considered	8 / 31 / 04	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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